REMARKS

Claims **1-16** are pending. Claims **9** and **11** are amended for grammatical reasons. Claims **21-23** are added for the Examiner's consideration. The above amendments and added claims do not add new matter to the application; and support for the amendment and added claims is found at least in Figure(s) 2(a) – 2(k) and at pages 5-13 of the specification. Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Objection to Claims

In the Office Action, the Examiner objected to claim **11** and suggested changing "HF" to --Hf--, since "Hf" is the recognized form of the element. In response, Applicants have amended claim 11 in accordance with the Examiner's suggestions, for the sole purpose of clarification, not for the purpose of avoiding prior art or narrowing the claimed invention. Thus, no change in claim scope is intended, and Applicants do not intend to relinquish any subject matter by this amendment. Applicants respectfully submit that claim 11, as amended, overcomes the stated objection. Accordingly, Applicants respectfully request withdrawal of the objection of claim 11.

35 U.S.C. § 112, second paragraph, Rejection

Claim 9 is rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as

the invention. Specifically, the Examiner suggested that the limitation "deposited oxide" in lines 1 and 2-3 had insufficient antecedent basis.

To provide proper antecedent basis, Applicants have amended claim 9 to recite the limitation "a deposited oxide" in line 1. This amendment is made for the sole purpose of clarification, not for the purpose of avoiding prior art or narrowing the claimed invention. Thus, no change in claim scope is intended, and Applicants do not intend to relinquish any subject matter by these amendments. Applicants respectfully submit that claim 9, as amended, fully complies with the requirements of 35 U.S.C. § 112, second paragraph. Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 112, second paragraph rejection of claim 9.

35 U.S.C. § 103 Rejection

Claims **1**, **3-5**, **12**, and **14-16** are rejected under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,288,694 issued to Doyle, *et al.* ("Doyle"). Claim **2** is rejected under 35 U.S.C. § 103(a) as being unpatentable over Doyle *et. al.,* in view of U. S. Patent No. 4,517,731 issued to Khan, *et al.* ("Khan"). Claims **1**, **3-16** are further rejected under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,204,103 issued to Bai, *et al.* ("Bai") in view of Doyle. These rejections are respectfully traversed.

In order to reject a claim under 35 U.S.C. §103(a), the MPEP mandates that three basic criteria must be met to provide a *prima facie* case of obviousness:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim

> limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claims 1 and 16

Claim 1 recites, in pertinent part:

> covering the p-type transistor with a mask; and
>
> oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor.

Claim 16 recites, in pertinent part:

> oxidizing a portion of a gate polysilicon of the n-type field effect transistor, such that tensile mechanical stresses are formed within a channel of the n-type field effect transistor, without creating additional tensile stresses in a channel of the p-type field effect transistor.

The Examiner suggests that Doyle, at Figures 5-7, column 4, lines 40-55, and at Figure 11, column 5, lines 5-25, discloses the elements recited in claims 1 and 16. Applicants respectfully disagree.

Doyle, at Figures 5-7, discloses creating voids *in a substrate* before either an n-type or a p-type transistor is formed. Additionally, at Figures 8-10, Doyle discloses creating voids within the *source and drain regions* of a substrate after an n-type or a p-type transistor is formed. Also, Doyle discloses, in Figures 11 – 13, creating voids *in a polysilicon gate* after an n-type or a p-type transistor is formed. In Figure 17, Doyle discloses a single void 142 formed in a channel

region. In Figure 18, Doyle discloses multiple voids 152 formed at the outer edges of a channel region.

In keeping with the teachings of Doyle as a whole, the single void 142 or the multiple voids 152 are not formed by oxidizing the polysilicon gate 149 and 159. Instead, they are implanted within the substrate before the gates 149 and 159 are formed. Specifically, Figures 5-7 and 11 disclose a method that directly implants one or more voids within a channel region before an n-type or a p-type device is formed. After this implantation, the gate is formed. However, there is no suggestion, whatsoever, of oxidizing a gate to form a stress in a channel.

In comparing the recited elements of claims 1 and 16 with Doyle, it is seen that Doyle's disclosures are entirely opposite the claimed invention. Claims 1 -14 recite oxidizing a polysilicon gate (not a substrate on which it rests, nor adjacent source and drain regions) to apply tensile mechanical stress a channel of an n-type transistor. As claims 1 and 16 recite, the tensile mechanical stress within the channel results from oxidation of the gate polysilicon, not from voids implanted into the substrate as taught by Doyle. Consequently, Doyle fails to disclose or suggest the claimed element of "oxidizing a portion of a *gate polysilicon* of the n-type transistor, such that tensile mechanical stresses are formed *within a channel* of the n-type transistor." For these reasons, Claims 1 and 16 are distinguishable over Doyle.

The Examiner further rejected claims 1 and 16 over the combination of Bai (U.S. Patent No.: 6,204,103) in view of Doyle. The Examiner noted that Bai discloses a method of forming an integrated circuit comprising a plurality of semiconductor devices including an n-type

transistor and a p-type transistor on a semiconductor wafer[1] , but the Examiner admitted at pages 5 and 6 of the Office Action, that neither Bai nor Doyle disclose the claimed elements of "covering a p-type transistor with a mask" and "oxidizing a portion of a gate polysilicon of the n-type field effect transistor, such that tensile mechanical stresses are formed within a channel of the n-type field effect transistor, without creating additional tensile stresses in a channel of the p-type field effect transistor." Nevertheless, the Examiner argues that such steps would have been obvious to one of ordinary skill in the art at the time the invention was made because Doyle teaches increasing the tensile stresses in a N-MOS region while preventing the increasing of tensile stresses in the PMOS region. Applicants respectfully disagree.

Given the teachings of Doyle and Bai (without the benefit of hindsight gleaned from Applicants' application), it would *not* have been obvious for one of ordinary skill in the art at the time the invention was made to mask a p-type transistor and to oxidize a gate polysilicon of a n-type transistor to increase tensile stresses in a channel of the n-type transistor. It would not have been obvious because the combination of Doyle and Bai expressly teaches creating voids in one of a gate, a channel, a source region, or a drain region of a n-type transistor, to create tensile stresses *in the particular element in which the voids are formed.* The claimed invention, in contrast, oxidizes the *polysilicon gate* of the n-type transistor to create tensile stresses in an *adjacent structure*, namely the channel of the n-type transistor. By illustrating and describing, at several points, a n-type transistor having an non-stressed (e.g., non-oxidized) polysilicon gate

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[1] Applicants do not dispute this general statement, but note that the method and resulting N-type and P-type transistors disclosed in Bai are very different from those recited in claims 1 and 16.

over top of a stressed channel having voids formed therein, the cited references expressly teach away from the elements recited in claims 1 and 16.

Additionally, the combination of Bai with Doyle would not produce the invention recited in claim 1. Instead, the combination of Bai and Doyle would produce a semiconductor wafer having one or more voids formed therein within one or more channel areas, and having a plurality of p-type (TiSi2) and n-type (MoSi2) transistors formed thereon. However, the tensile stresses applied to n-type transistors would be caused by the voids themselves, and not by forces exerted by an oxidized polysilicon gate. Again, this is contrary to the claimed invention.

For these reasons, claims 1 and 16 are allowable over the Bai and Doyle, whether alone or in combination. Accordingly, allowance of claims 1 and 16 is respectfully requested.

Claims 2-15

Claims 2-15 are allowable over the cited reference based on their dependencies from an allowable base claim. Additionally, claims 14 and 15 are further allowable based on their additional features.

Claim 14 recites, in pertinent part:

> wherein the step of oxidizing comprises oxidizing the gate polysilicon of the n-type field effect transistor to create a stress of about 700MPa in a channel of the n-type field effect transistor.

Claim 15 recites, in pertinent part:

> wherein the step of oxidizing comprises oxidizing the gate polysilicon of the n-type field effect transistor to create tensile mechanical stresses are about 500Pa to about 1000Pa.

The Examiner submits that the claimed tensile stress ranges lack criticality because the Applicants do not teach that the tensile stress ranges solve any stated problem or are for any particular purpose. Applicants respectfully traverse this submission, and direct the Examiner's attention to Figures 4 and 5, as well as to page 2 of the specification, where it is stated that tensile stresses in conventional n-type devices are relatively moderate (i.e., for example, about 200 MPa to about 300 MPa). Comparing the results of Figures 4 and 5 to these conventional results, it is seen that embodiments of the present invention offer improved tensile stress ranges, which are in embodiments are critical to their operation. Additionally, Applicants further direct the Examiner's attention to page 10 of the specification, where it is noted:

> the oxidation of the gate of the NFETs creates large tensile stresses in the channel region of the NFETs ... Further, these tensile stresses increase electron mobility along the channel, and improve the performance of the NFETs.

At page 13, it is noted that the desired stresses are tensile and add values of the order of 200MPa and above. For these reasons, and because the cited references disclose a tensile stress of about 100 MPa, the tensile stress ranges recited in claims 14 and 15 are allowable. Consequently, allowance of claims 14 and 15 is respectfully requested.

Added Claims

Added claims 21-23 are directed to reciting additional elements that distinguish over the cited references. Claims 21-23 are allowable based on their dependencies from allowable base claim 1. Additionally, none of their recited features are disclosed by Doyle, Bai, or Khan,

whether alone or in combination. Accordingly, allowance of claims 21-23 is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to **IBM Deposit Account No. 09-0458**.

Respectfully submitted,

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